Silicon-on-Insulator (SOI) Switches for Cellular and WLAN Front-End Applications

WSO: Advancements in Front End Modules for Mobile and Wireless Applications

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**Acknowledgements**

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Outline

• Motivation and Cellular Switch Considerations
• Switch Technology Overview
• SOI Switch Examples
• Design of High Order Switches on SOI
• Nonlinearities, Harmonics and IMD
• Spurious Emissions and ESD Considerations
• Conclusions
Ever increasing need for higher data rates drives the standards to those of 3G / 4G.

Market share and volume of 3G / 4G handsets expected to increase tremendously.

Many bands and band combinations considered for 3G / 4G handsets to roam at different regions.
• 3G / 4G system architectures require a complex integration of switch, filter, and duplex functions in the front-end.
High Power Switch Considerations

- PA output power often represented by ~36 dBm source
- Antenna port impedance varies greatly
  - Operating VSWR up to 5:1, functional into 20:1
- Off-state switch must stand-off high AC voltages
  - Maintain Reliability
  - Linearity
- For most IC technologies, several FETs must be stacked in series
What is SOI?

- SOI = Silicon-on-Insulator
- Thin layer of Si / Buried Oxide / Handle Wafer
- Created using wafer bonding and ion implantation cleaving process
- SOI (on high resistivity substrates) decouples FET body terminals, enabling device stacking for high power switch applications
Thick and Thin-Film SOI

**Thick-film SOI**
- Device layer thickness > S/D junction depth
- Device operation similar to bulk Si
- Circuit blocks can be transferred from bulk Si with minimal changes

**Thin-film SOI**
- S/D doping extends to buried oxide → reduced S/D capacitance (Coff)
- More extensive re-design needed for existing circuit blocks
Switch Figure of Merit

• “Figure of merit”: trade off between insertion loss (resistance) and isolation (capacitance)

• FOM is a device size independent measure of how good a switch device/technology is.

• Lower FOM is better.

FOM = Ron * Coff
### Switch Technology Comparison

<table>
<thead>
<tr>
<th>Process</th>
<th>Device</th>
<th>Ron [Ω-mm]</th>
<th>Coff [fF/mm]</th>
<th>Ron*Coff [fs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFMD FET1H pHEMT</td>
<td>1 single gate</td>
<td>1.4</td>
<td>160</td>
<td>224</td>
</tr>
<tr>
<td>RFMD FET1H pHEMT</td>
<td>Two series triple gate</td>
<td>0.9</td>
<td>300</td>
<td>270</td>
</tr>
<tr>
<td>0.18um thick-film SOI</td>
<td>5V NFET Lg=0.6um 13.0nm gate ox</td>
<td>1.9</td>
<td>255</td>
<td>485</td>
</tr>
<tr>
<td>0.18um thin-film SOI</td>
<td>2.5V NFET Lg=0.32um 5.2nm gate ox</td>
<td>0.8</td>
<td>310</td>
<td>250</td>
</tr>
<tr>
<td>0.25um SOS</td>
<td>NFET 5.0nm gate ox</td>
<td>1.6</td>
<td>280</td>
<td>448</td>
</tr>
<tr>
<td>0.35um SOS</td>
<td>Source: “Single chip phone RF is possible”, Electronics Weekly, February 14, 2012.</td>
<td></td>
<td></td>
<td>253</td>
</tr>
</tbody>
</table>

- 0.18um thin-film SOI offers Ron*Coff similar to pHEMT / SOS.
- Integrated switch controller in the SOI die possible.
Switch Branch and Resistor Dimensioning

- Use enough number of stacks to handle the specified power.
- Device width should be just right to meet the insertion loss/isolation specifications.
  - Wider widths result in poor isolation, and narrower widths result in poor insertion loss.
- The gate resistors should be large enough to float the gate, but small enough to have adequate switching time.
- Resistors between source and drain used to provide 0 V DC bias to S/D of devices. No DC blocking caps needed on RF ports.

\[
R_{gate} \gg \frac{1}{2\pi f (C_{gs} + C_{gd})}
\]
Switch Timing Considerations

- Large signal switching event shown for a WLAN switch that requires stringent switching times in the order of 100 nsec small signal, 500 nsec large signal (Full Power).

- Accomplished by measuring the time between the time the control bit applied and the time of a 900 MHz 29 dBm RF signal stabilize in a spectrum analyzer.

- Fundamental reaches full power at 60+180 = ~240 nsec, well below 500 nsec requirement!

- No significant variation observed vs. voltage, temperature.
An RF switch includes multiple series and shunt branches and a controller that would provide the necessary bias voltages to the switch devices for a given control bit setting.

In an equivalent circuit model, ON devices can be considered as resistors, OFF devices as capacitors.
Example: SP9T Switch for Switch Duplexer Module Applications

- SOI integrates the controller and RF section in a single die vs. pHEMT having a complex two die solution.
- Wire bond and flip chip SOI SP9T switches designed for an SDM application.
  - 2 high power GSM TX,
  - 3 high power WCDMA, and
  - 4 low power GSM RX ports.
At 915 MHz, TX and TRX ports have 0.45 dB, RX ports have 0.55 dB insertion loss.

At 1990 and 2170 MHz, insertion losses increase by about 0.2 and 0.25 dB, respectively.

No intentional matching employed, hence less insertion loss achievable with matching.
• TX / TRX to TX / TRX isolation better than 29 dB up to 2170 MHz.

• Lower isolation to one branch due to higher branch-to-antenna and bond wire coupling. Other combinations achieve better than 34 dB isolation up to 2170 MHz.

• Higher isolation achievable with flip-chip SP9T.
• TX / TRX to RX isolation better than 32 dB up to 2170 MHz.
• Adjacent TRX / RX and closer RX / ANT combination achieve lower isolation compared to the rest due to higher branch-to-branch and bond wire coupling.
• Higher isolation achievable with flip-chip SP9T.
RX to RX Isolation

- RX to RX isolation better than 28 dB up to 2170 MHz.
- Adjacent branches achieve lower isolation compared to other combinations due to higher branch-to-branch and bond wire coupling.
- Higher isolation achievable with flip-chip SP9T.
• Equivalent circuit model for a symmetric SP16T in one of the active modes shown above.

• 0.32 um channel length series and shunt devices assumed. Shunt device size fixed at 1mm.

• Let’s study the effect of series branch size on insertion loss and isolation at 915, 1910, and 2690 MHz.
Branch Size Study for High Order Switches (SP16T)

- Return loss increases significantly and degrades insertion loss with increased series branch size. It must be tuned!
- There exists an optimum branch size to give lowest insertion loss if you can match!
Matching Values for SP16T

- Use series L shunt C to match capacitive loading at antenna.
- Different matching values needed at different frequencies!
- Choose your device size considering insertion loss/isolation specs and matching!
Example: Design of a Single Chip SOI MIPI Switch System

- Single die flip chip solution for a SP7T+SP5T+SP3T+SP3T switch system with MIPI interface having 50+ switch states.
- Switch die size = 3 x 1.2 mm$^2$.
- 5 layer evaluation laminate designed to test and tune the switches.
# Measured Insertion Loss

<table>
<thead>
<tr>
<th>Switch</th>
<th>Mode</th>
<th>Max. Frequency (MHz)</th>
<th>Insertion Loss (MHz)</th>
<th>Insertion Loss (dB)</th>
<th>Return Loss (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB SP3T</td>
<td>Mode 1</td>
<td>849</td>
<td>0.30</td>
<td>0.27</td>
<td>29</td>
</tr>
<tr>
<td>LB SP3T</td>
<td>Mode 2</td>
<td>915</td>
<td>0.30</td>
<td>0.29</td>
<td>34</td>
</tr>
<tr>
<td>LB SP3T</td>
<td>Mode 3</td>
<td>862</td>
<td>0.30</td>
<td>0.3</td>
<td>28</td>
</tr>
<tr>
<td>HB SP3T</td>
<td>Mode 4</td>
<td>1980</td>
<td>0.35</td>
<td>0.41</td>
<td>27</td>
</tr>
<tr>
<td>HB SP3T</td>
<td>Mode 5</td>
<td>1755</td>
<td>0.30</td>
<td>0.35</td>
<td>32</td>
</tr>
<tr>
<td>HB SP3T</td>
<td>Mode 6</td>
<td>1910</td>
<td>0.35</td>
<td>0.41</td>
<td>34</td>
</tr>
<tr>
<td>LB SP5T</td>
<td>Mode 7</td>
<td>915</td>
<td>0.40</td>
<td>0.35</td>
<td>32</td>
</tr>
<tr>
<td>LB SP5T</td>
<td>Mode 8</td>
<td>894</td>
<td>0.40</td>
<td>0.45</td>
<td>32</td>
</tr>
<tr>
<td>LB SP5T</td>
<td>Mode 9</td>
<td>960</td>
<td>0.40</td>
<td>0.49</td>
<td>32</td>
</tr>
<tr>
<td>LB SP5T</td>
<td>Mode 10</td>
<td>960</td>
<td>0.40</td>
<td>0.45</td>
<td>29</td>
</tr>
<tr>
<td>LB SP5T</td>
<td>Mode 11</td>
<td>960</td>
<td>0.50</td>
<td>0.51</td>
<td>31</td>
</tr>
<tr>
<td>HB SP7T</td>
<td>Mode 12</td>
<td>1910</td>
<td>0.50</td>
<td>0.46</td>
<td>16</td>
</tr>
<tr>
<td>HB SP7T</td>
<td>Mode 13</td>
<td>1990</td>
<td>0.50</td>
<td>0.59</td>
<td>14</td>
</tr>
<tr>
<td>HB SP7T</td>
<td>Mode 14</td>
<td>2170</td>
<td>0.55</td>
<td>0.72</td>
<td>14</td>
</tr>
<tr>
<td>HB SP7T</td>
<td>Mode 15</td>
<td>2690</td>
<td>0.60</td>
<td>0.75</td>
<td>13</td>
</tr>
<tr>
<td>HB SP7T</td>
<td>Mode 16</td>
<td>1880</td>
<td>0.50</td>
<td>0.74</td>
<td>12</td>
</tr>
<tr>
<td>HB SP7T</td>
<td>Mode 17</td>
<td>1910</td>
<td>0.50</td>
<td>0.7</td>
<td>12</td>
</tr>
<tr>
<td>HB SP7T</td>
<td>Mode 18</td>
<td>2690</td>
<td>0.60</td>
<td>0.71</td>
<td>12</td>
</tr>
</tbody>
</table>

- Insertion loss targets achieved in LB SP3T switch.
- Up to ~0.05 dB higher loss in HB SP3T switch.
- [-0.05,0.10] dB around the design targets achieved in LB SP5T switch.
- [-0.05,0.20] dB around the design targets achieved in HB SP7T switch. But, by further tuning the mismatch, some of the mismatch loss can be recovered.
A parasitic conduction layer may form at Si/SiO$_2$ interface below SOI buried oxide.

A structure (metal trace or device) above the oxide with varying potential may modulate the conductive characteristic at the interface, creating a non-linear impedance.

This limited the linearity of SOI switches, but this issue has been solved now, making SOI a viable high power switch technology.

Measured Harmonic Distortion

- Low Band 2fo and 3fo better than -58 and -47 dBm up to 37 dBm input power, respectively.
- High Band 2fo and 3fo better than -49 and -46 dBm up to 36 dBm input power, respectively.
- Measured harmonic levels considerably better than most antenna/mode switch specifications.
SOI Switch Model vs. Measurement Comparison

- Simulations can predict measured small signal and large signal performance
  - Assures new designs hit performance targets
  - Enables module co-design with proper matching
Switch Linearity Requirements

- Typical IMD specification is -105 dBm.
- Adequate IMD levels measured for the UMTS ports as shown below.
- IMD 45 / IMD 190 improved to a sufficient level with the shunt ESD inductor on the SDM.

* T. Ranta et. al., 2005.

<table>
<thead>
<tr>
<th>TX Frequency (F1), MHz</th>
<th>Blocker Frequency (F2), MHz</th>
<th>Distortion Type</th>
<th>IMD (RX) Frequency, MHz</th>
<th>Measured SP9T IMD, dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1950</td>
<td>1760</td>
<td>2F1-F2</td>
<td>2140</td>
<td>-119</td>
</tr>
<tr>
<td>1950</td>
<td>4090</td>
<td>F2-F1</td>
<td>2140</td>
<td>-110</td>
</tr>
<tr>
<td>1950</td>
<td>190</td>
<td>F1+F2</td>
<td>2140</td>
<td>-106</td>
</tr>
<tr>
<td>836.5</td>
<td>791.5</td>
<td>2F1-F2</td>
<td>881.5</td>
<td>-122</td>
</tr>
<tr>
<td>836.5</td>
<td>1718</td>
<td>F2-F1</td>
<td>881.5</td>
<td>-120</td>
</tr>
<tr>
<td>836.5</td>
<td>45</td>
<td>F1+F2</td>
<td>881.5</td>
<td>-102</td>
</tr>
</tbody>
</table>
Spurious Emissions

• Measured RX mode spurious emissions better than -123 dBm.
• Measured RX band noise better than -97 dBm ($f_{TX} = 915$ MHz, $P_{TX} = 35$ dBm).
ESD Considerations

- Controller must be protected using appropriate ESD diodes and clamp circuits.
- In the RF section, utilization of shunt branches offer very good ESD protection up to 2 kV HBM.
- The mechanism for shunting the ESD current to ground is believed to be that the gate of the shunt branches couple up through capacitive coupling with the large ESD voltage transient. This effectively turns the shunt transistors on giving the ESD energy a path to ground.
SOI Performance Snapshot

Implementation Ease (TX Port Impedance)

Size

Cost

Insertion Loss

Isolation

Harmonics

Id ($\mu$A)

IMD

800+

100

50

Competitor A

Competitor B

SOI

RFMD
Conclusions

• 3G / 4G smart handsets will dominate the market in the next few years, which opens a great opportunity for front-end suppliers.

• High resistivity SOI enables FET stacking, allowing the design of high power antenna / mode switches.

• Low RON*COFF product results in competitive switch insertion loss and isolation performance.

• High resistivity SOI substrate linearity issues solved, enabling the design of high throw count SOI antenna switches with excellent harmonic and intermodulation distortion performance.

• Adequate levels of TX and RX mode spurious emissions measured.

• 2000 V Human Body Model (HBM) ESD tolerance achieved on the RF ports (no blocking capacitors on the ports).