

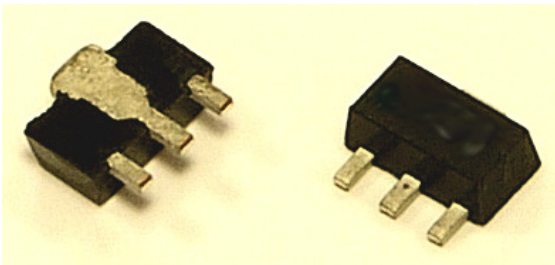


Product Description

The FPD750SOT89CE is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It features a 0.25µm×1500µm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure is designed for improved linearity over a range of bias conditions and input power levels.

Optimum Technology Matching® Applied

- GaAs HBT
- GaAs MESFET
- InGaP HBT
- SiGe BiCMOS
- Si BiCMOS
- SiGe HBT
- GaAs pHEMT
- Si CMOS
- Si BJT
- GaN HEMT
- InP HBT
- RF MEMS
- LDMOS



Features

- 25dBm Output Power (P1dB)
- 18dB Small-Signal Gain (SSG)
- 0.6dB Noise Figure
- 39dBm OIP₃
- 55% Power-Added Efficiency
- FPD750SOT89CE: RoHS Compliant (Directive 2002/95/EC)

Applications

- Drivers or Output Stages in PCS/Cellular Base Station Transmitter Amplifiers
- High Intercept-point LNAs
- WLL, WLAN, and Other Types of Wireless Infrastructure Systems.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
P _{1dB} Gain Compression	23	25		dBm	V _{DS} =5V, I _{DS} =50% I _{DSS}
Small-Signal Gain (SSG)	16.5	18		dB	V _{DS} =5V, I _{DS} =50% I _{DSS}
PAE		50		%	V _{DS} =5V, I _{DS} =50% I _{DSS} , P _{OUT} =P _{1dB}
Noise Figure (NF)		0.8	1.0	dB	V _{DS} =5V, I _{DS} =50%
		0.6		dB	V _{DS} =5V, I _{DS} =25%
OIP ₃	36	38		dBm	V _{DS} =5V, I _{DS} =50% I _{DSS} . Matched for optimal power.
		39		dBm	Matched for best IP ₃
Saturated Drain-Source Current (I _{DSS})	185	230	280	mA	V _{DS} =1.3V, V _{GS} =0V
Maximum Drain-Source Current (I _{MAX})		375		mA	V _{DS} =1.3V, V _{GS} ≈+1V
Transconductance (GM)		200		ms	V _{DS} =1.3V, V _{GS} =0V
Gate-Source Leakage Current (IGSO)		1	15	µA	V _{GS} =-5V
Pinch-Off Voltage (V _p)	0.7	1.0	1.3	V	V _{DS} =1.3V, I _{DS} =0.75mA
Gate-Source Breakdown Voltage (V _{BDS})	12	16		V	I _{GS} =0.75mA
Gate-Drain Breakdown Voltage (V _{BDD})	12	16		V	I _{GD} =0.75mA
Thermal Resistivity (θJC) *		83		°C/W	

*Note: T_{AMBIENT}=22 °C, RF specifications measured at f=1850MHz using CW signal (except as noted).

Absolute Maximum Ratings¹

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS}) ($-3V < V_{GS} < 0.5V$)	8	V
Gate-Source Voltage (V_{GS}) ($0V < V_{DS} < +8V$)	-3	V
Drain-Source Current (I_{DS}) (For $V_{DS} > 2V$)	I_{DSS}	
Gate Current (I_G) (Forward or reverse)	7.5	mA
RF Input Power (P_{IN}) ² (Under any acceptable bias state)	175	mW
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-55 to 150	°C
Total Power Dissipation (P_{TOT}) ^{3,4}	1.8	W
Gain Compression (Under bias conditions)	5	dB
Simultaneous Combination of Limits ⁵ (2 or more max. limits)		

Notes:

¹ $T_{AMBIENT} = 22\text{ °C}$ unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.

²Max. RF input limit must be further limited if input VSWR > 2.5:1.

³Users should avoid exceeding 80% of 2 or more Limits simultaneously.

⁴Total Power Dissipation (P_{TOT}) defined as $(P_{DC} + P_{IN}) - P_{OUT}$, where P_{DC} : DC Bias Power, P_{IN} : RF Input Power, P_{OUT} : RF Output Power.

Total Power Dissipation to be de-rated as follows above 22 °C:

$P_{TOT} = 1.8 - (0.012\text{ W/°C}) \times T_{PACK}$, where T_{PACK} = source tab lead temperature above 22 °C. (Coefficient of de-rating formula is Thermal Conductivity.)

Exampe: For a 65 °C carrier temperature: $P_{TOT} = 1.8\text{ W} - (0.012 \times (65 - 22)) = 1.28\text{ W}$



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

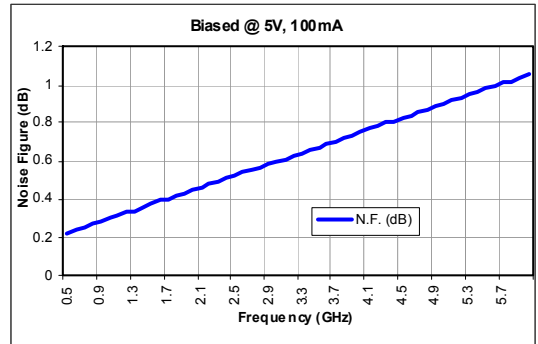
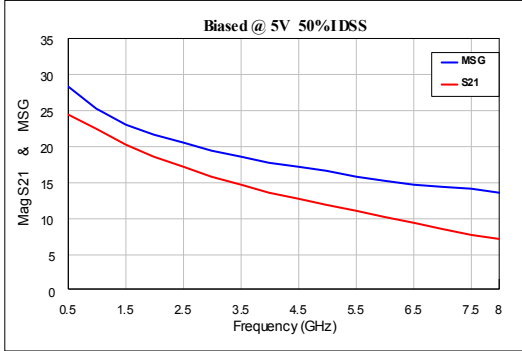
Biassing Guidelines

Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that gate bias is applied before drain bias, otherwise the pHEMT may be induced to self-oscillate.

Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.

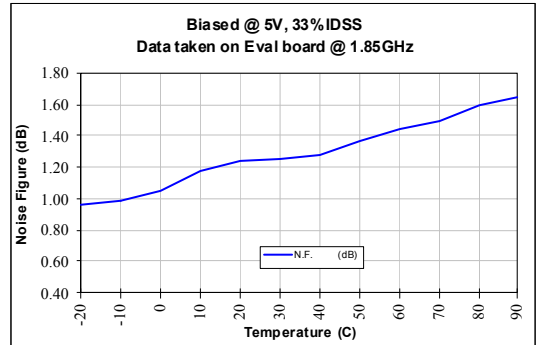
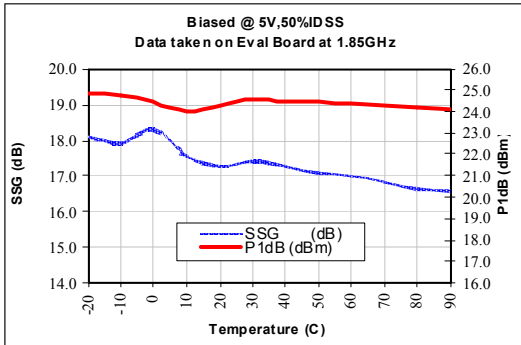
For standard Class A operation, an operating point of 50% of I_{DSS} is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. A class A/B Bias of 25% to 33% of I_{DSS} to achieve better OIP₃ and Noise Figure performance is suggested.

Frequency Response



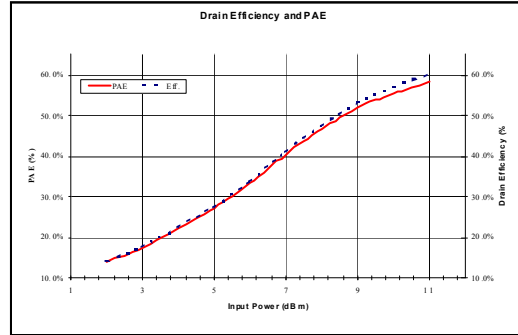
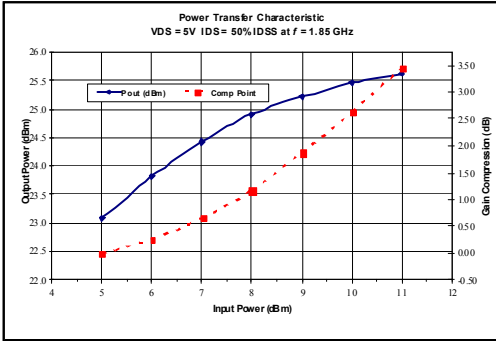
Note: Device tuned for minimum noise figure.

Temperature Response

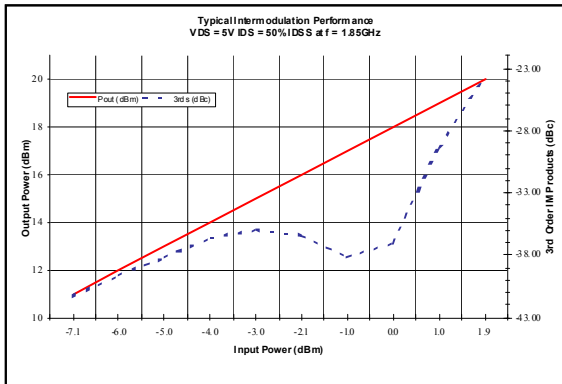


Note: Data taken on evaluation board tuned for maximum power. Achievable noise figure is lower when optimized.

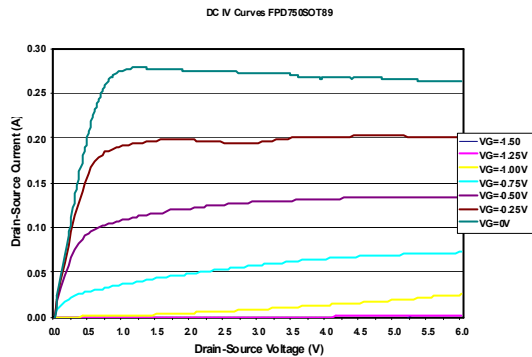
Typical Tuned RF Performance



Note: Typical power and efficiency is shown above. The devices were biased nominally at $V_{DS}=5V$, $I_{DS}=50\%$ of I_{DSS} , at a test frequency of 1.85GHz. The test devices were tuned (input and output tuning) for maximum output power at 1dB gain compression.



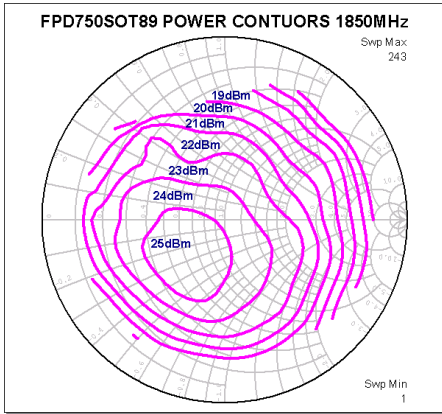
Note: pHEMT devices have enhanced intermodulation performance. This yields OIP3 values of about P1dB+14dBm. This IMD enhancement is affected by the quiescent bias and the matching applied to the device.



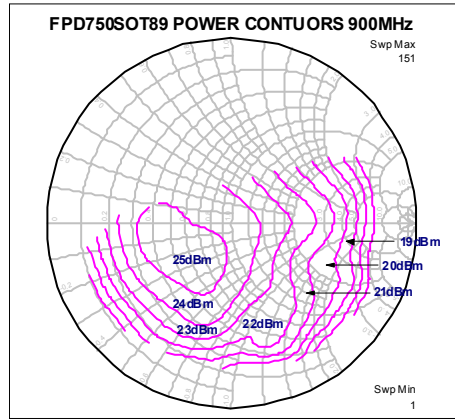
Note: The recommended method for measuring I_{DSS} or any particular I_{DS} , is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the $V_{DS} > 1.3V$ will generally cause errors in the current measurements, even in stabilized circuits.

Typical Output Plane Power Contours

($V_{DS}=5V, I_{DS}=50\% I_{DSS}$)



1850 MHz



900 MHz

Contours swept with a constant input power, set so that optimum P1dB is achieved at the point of output match.

Input (Source plane) Γ's:

$0.50 \angle 142.8^\circ$

$0.37 + j0.35$ (normalized)

$18.5 - j17.5 \Omega$

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

Contours swept with a constant input power, set so that optimum P1dB is achieved at the point of output match.

Input (Source plane) Γ's:

$0.79 \angle 36.9^\circ$

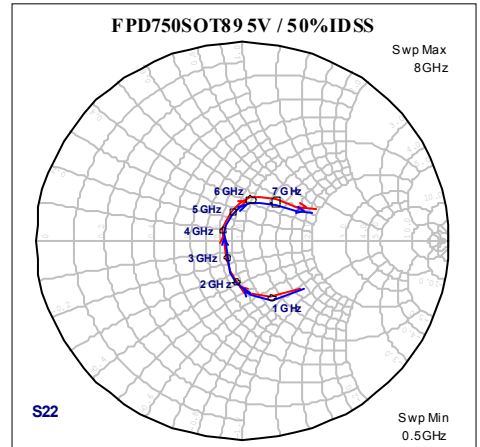
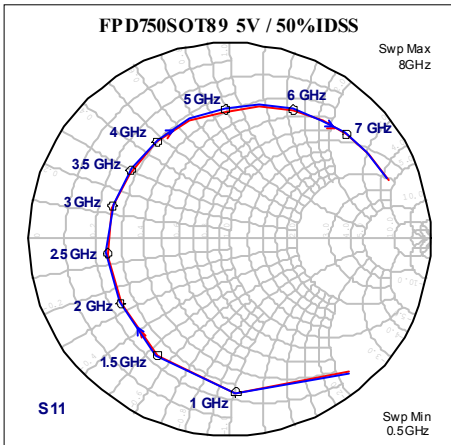
$1.0 + j2.6$ (normalized)

$50 + j130 \Omega$

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

Typical Scattering Parameters

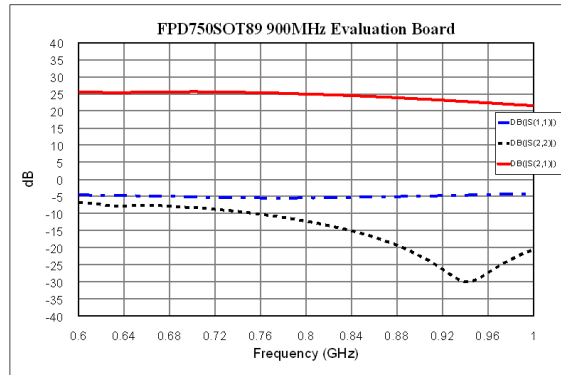
(50Ω System)



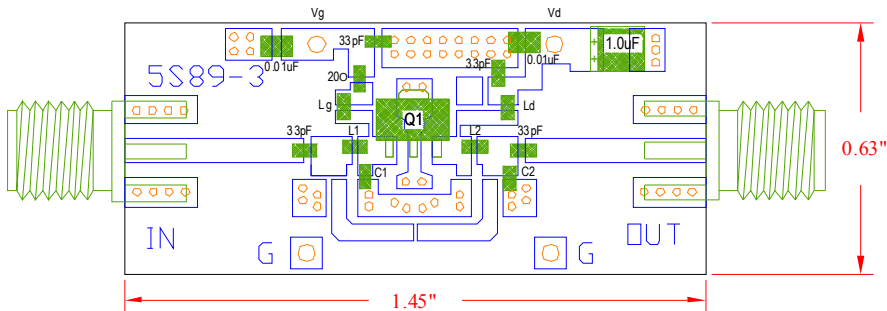
Reference Design (0.9 GHz)

Parameter	Typical	Unit
Gain	23	dB
P1dB	23.5	dBm
OIP ₃	35	dBm
NF	0.6	dB
S ₁₁	-5	dB
S ₂₂	-20	dB
V _D	5	V
V _G	-0.4 to -0.6	V
I _D	100	mA

Note: OIP₃ measured at 10dBm per tone.



Evaluation Board Layout

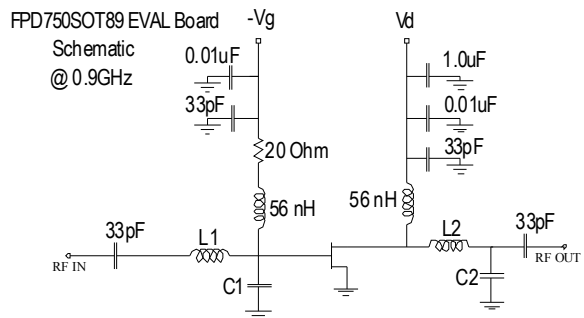


Component Values

Component	Value	Description
L _g	56 nH	LL 1608 Toko chip inductor
L _d	56 nH	LL 1608 Toko chip inductor
L ₁	12 nH	LL 1608 Toko chip inductor
L ₂	6.8 nH	LL 1608 Toko chip inductor
C ₁	0.5 pF	ATC 600S chip capacitor
C ₂	1.2 pF	ATC 600S chip capacitor

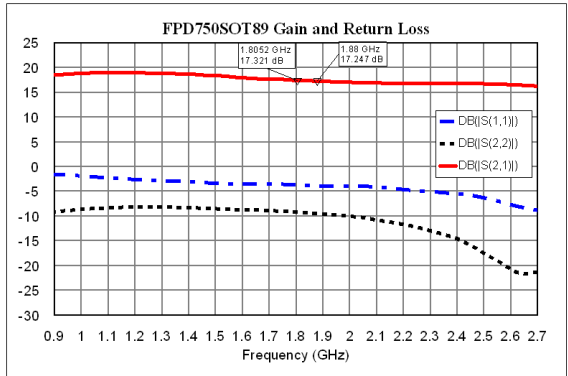
Evaluation board material: 31mil thick FR4 with 1/2 oz. Cu on both sides.

DC-blocking capacitors are ATC series 600S. A tantalum 1.0μF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.



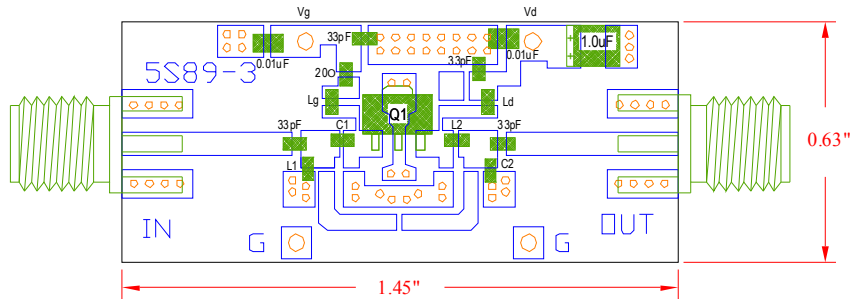
Reference Design (1.85 GHz)

Parameter	Typical	Unit
Gain	17.2	dB
P1dB	24	dBm
OIP ₃	35	dBm
NF	0.7	dB
S11	-5	dB
S22	-10	dB
V _D	5	V
V _G	-0.4 to -0.6	V
I _D	100	mA



Note: OIP₃ measured at 10dBm per tone.

Evaluation Board Layout

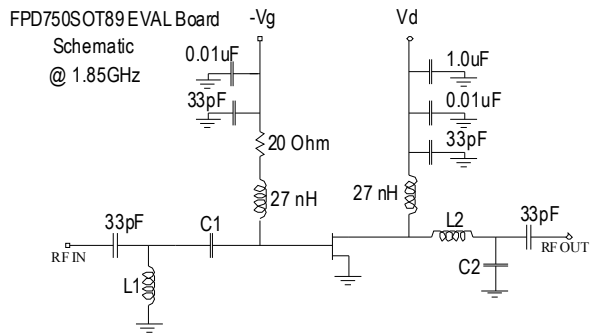


Component Values

Component	Value	Description
Lg	27 nH	LL 1608 Toko chip inductor
Ld	27 nH	LL 1608 Toko chip inductor
L1	6.8 nH	LL 1608 Toko chip inductor
L2	1.8 nH	LL 1608 Toko chip inductor
C1	2.7 pF	ATC 600S chip capacitor
C2	0.5 pF	ATC 600S chip capacitor

Evaluation board material: 31mil thick FR4 with 1/2oz. Cu on both sides.

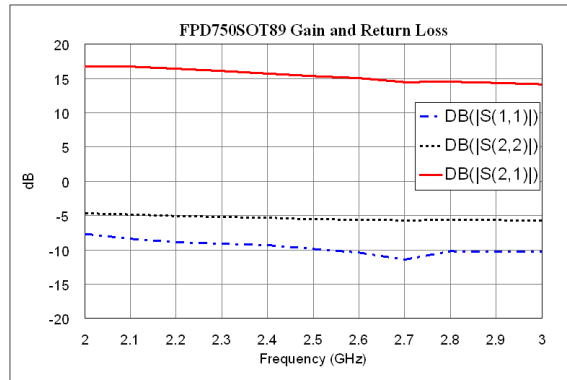
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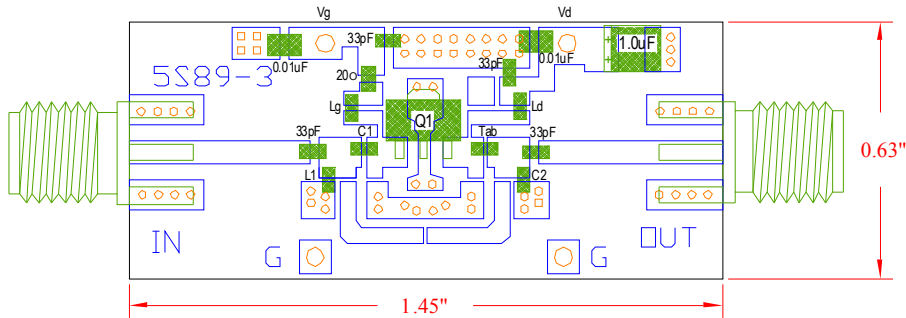
Reference Design (2.4GHz to 2.6GHz)

Frequency	2.4	2.5	2.6	Unit
SSG	15.4	15.2	15.0	dB
P1dB	24.3	24.3	24.4	dBm
OIP ₃	34.0	35.0	34.0	dBm
NF	0.95	0.95	1.0	dB
S ₁₁	-5.0	-5.5	-6.0	dB
S ₂₂	-9.5	-10.0	-10.0	dB
V _D	5			V
V _G	-0.4 to -0.6			V
I _D	100			mA

Note: OIP₃ measured at 10dBm per tone.



Evaluation Board Layout

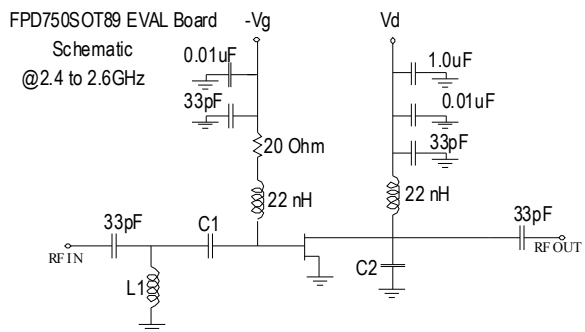


Component Values

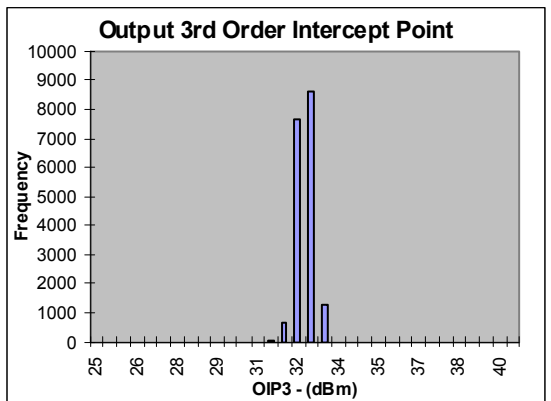
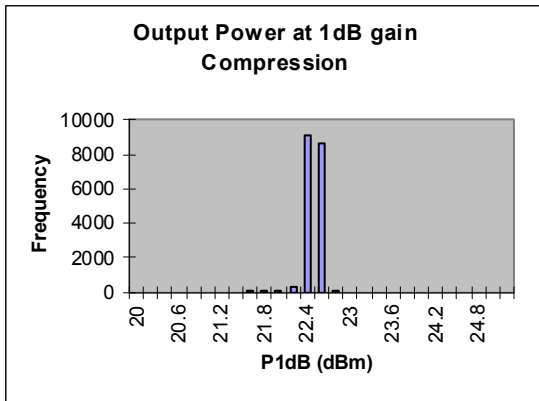
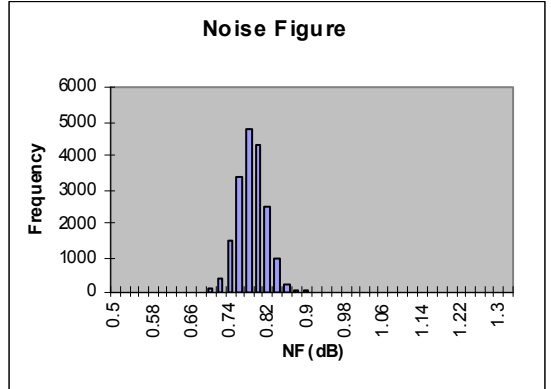
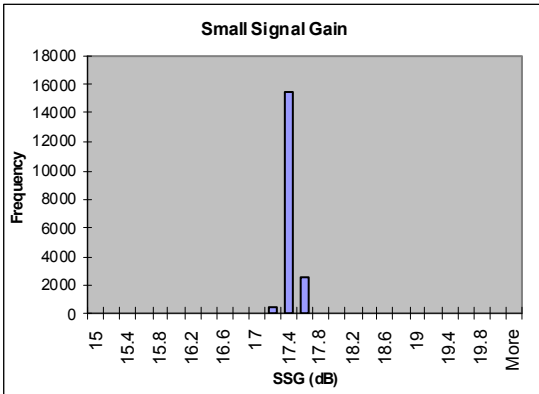
Component	Value	Description
L _g	22nH	LL 1608 Toko chip inductor
L _d	22nH	LL 1608 Toko chip inductor
L ₁	8.2nH	LL 1005 Toko chip inductor
C ₁	2.0pF	ATC 600S chip capacitor
C ₂	0.8pF	ATC 600S chip capacitor
Tab		Copper tab (no component)

Evaluation board material: 31mil thick FR4 with 1/2oz. Cu on both sides.

DC-blocking capacitors are ATC series 600S. A tantalum 1.0μF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.



Statistical Sample of RF Performance

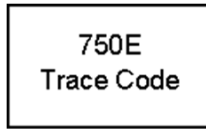


Note: The devices were tested by a high-speed automatic test system in a matched circuit based on an evaluation board design. This circuit is a dual-bias, single-pole, low-pass topology, and the devices were biased at $V_{DS}=4.0V$, $I_{DS}=100mA$, test frequency=2.0GHz.

S-Parameters (Biased @ 5V, 50% I_{DSS})

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.050	0.998	-5.6	19.465	172.4	0.003	94.4	0.448	-8.1
0.300	0.959	-30.9	16.931	154.5	0.016	77.5	0.438	-20.6
0.550	0.868	-52.5	15.126	137.7	0.028	64.7	0.406	-37.7
0.800	0.809	-72.3	13.452	124.3	0.038	55.2	0.379	-51.8
1.050	0.755	-90.2	12.024	112.1	0.046	47.2	0.352	-64.3
1.300	0.713	-106.5	10.762	101.4	0.052	40.7	0.324	-74.4
1.550	0.679	-121.5	9.707	91.8	0.057	35.1	0.294	-83.0
1.800	0.653	-135.6	8.828	82.7	0.062	29.2	0.267	-91.1
2.050	0.634	-148.8	8.080	74.1	0.066	24.3	0.241	-98.8
2.300	0.62	-161.8	7.441	66.0	0.069	19.4	0.214	-106.3
2.550	0.613	-173.5	6.890	58.1	0.073	14.9	0.188	-115.6
2.800	0.603	-175.0	6.407	50.2	0.076	10.5	0.169	-125.9
3.050	0.611	164.6	5.948	43.0	0.078	6.0	0.14	-140.7
3.300	0.614	154.5	5.557	35.7	0.080	2.2	0.123	-156.6
3.550	0.619	145.1	5.194	28.7	0.082	-2.4	0.113	-175.2
3.800	0.627	136.2	4.873	21.9	0.084	-6.0	0.11	164.9
4.050	0.636	127.9	4.594	15.4	0.085	-10.3	0.114	146.6
4.300	0.659	119.7	4.345	8.8	0.086	-13.3	0.133	132.4
4.550	0.663	110.6	4.138	1.8	0.089	-17.5	0.138	115.2
4.800	0.666	104.1	3.892	-4.8	0.090	-21.4	0.153	107.8
5.050	0.68	96.9	3.690	-11.0	0.091	-25.1	0.167	99.7
5.300	0.695	89.7	3.511	-17.4	0.092	-29.2	0.182	92.6
5.550	0.706	82.6	3.342	-23.7	0.093	-32.6	0.196	85.4
5.800	0.719	75.9	3.190	-30.1	0.094	-36.8	0.208	78.5
6.050	0.732	69.2	3.041	-36.5	0.095	-41.0	0.222	71.6
6.300	0.741	62.7	2.898	-42.8	0.096	-45.1	0.237	65.0
6.550	0.754	56.9	2.766	-49.1	0.096	-49.1	0.252	58.0
6.800	0.766	51.1	2.634	-55.3	0.095	-53.0	0.27	51.3
7.050	0.779	45.4	2.507	-61.6	0.095	-57.4	0.291	44.6
7.300	0.793	39.9	2.387	-67.8	0.095	-61.4	0.314	38.5
7.550	0.809	34.4	2.267	-73.9	0.093	-65.7	0.337	33.2
7.800	0.823	28.9	2.151	-79.9	0.092	-70.0	0.363	28.4
8.050	0.839	23.6	2.036	-85.7	0.091	-74.0	0.387	24.3
8.300	0.851	18.8	1.925	-91.3	0.089	-78.3	0.412	20.3
8.550	0.86	14.2	1.825	-96.7	0.087	-81.9	0.436	17.1
8.800	0.871	9.8	1.728	-102.0	0.084	-85.5	0.457	14.0
9.050	0.881	5.7	1.640	-106.9	0.083	-89.4	0.477	11.0
9.300	0.889	2.0	1.563	-111.8	0.082	-93.9	0.496	8.6
9.550	0.895	-1.5	1.494	-116.6	0.081	-98.4	0.514	6.0
9.800	0.904	-4.6	1.433	-121.2	0.080	-101.8	0.531	3.1
10.050	0.913	-8.3	1.384	-126.5	0.078	-107.1	0.548	-0.1
10.300	0.909	-12.0	1.323	-132.0	0.075	-111.9	0.552	-3.6
10.550	0.903	-15.2	1.264	-136.8	0.074	-116.6	0.557	-6.7

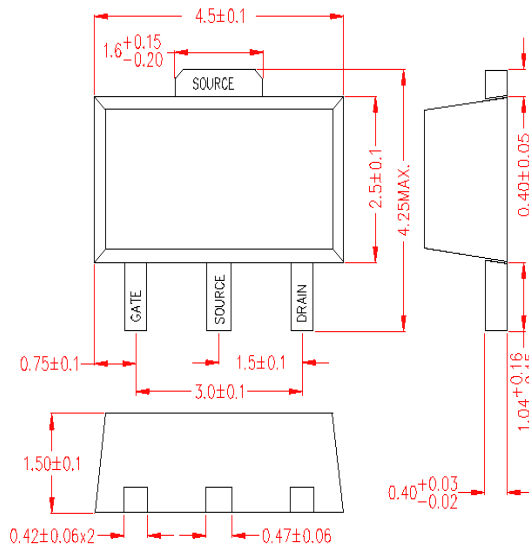
Part Identification



Trace Code to be assigned by SubCon

Package Outline

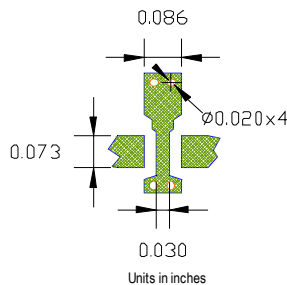
Dimensions in millimeters (mm)



Tape Dimensions and Part Orientation

Tape & Reel on this material is in accordance to EIA-481-1 except where exceptions are identified.

Device Footprint



Preferred Assembly Instructions

This package is compatible with both lead-free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260 °C.

Handling Precautions



To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 AND MIL-HDBK-263.

MSL Rating

The device has an MSL rating of Level 2. To determine this rating, preconditioning was performed to the device per the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, Moisture/Reflow sensitivity classification for non-hermetic solid state surface mount devices.

Application Notes and Design Data

Application Notes and design data including S-parameters, noise parameters, and device model are available on request from www.rfmd.com.

Reliability

An MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Description	Ordering Code
RoHS-Compliant Packaged pHEMT with enhanced passivation (recommended for new designs)	FPD750SOT89E
Packaged pHEMT evaluation board (2.0GHz)	FPD750SOT89PCK

Delivery Quantity	Ordering Code
Reel of 1000	FPD750SOT89E
Reel of 100	FPD750SOT89ESR
Bag of 25	FPD750SOT89ESQ
Bag of 5	FPD750SOT89ESB