IQ Modulator Programming Guide

Covers the following products:
RFMD2080 and RFMD2081

RFMD Multi-Market Products Group

REVISION HISTORY

Version	Date	Description of change(s)	Author(s)
0.1	02-May-11	Prep for Publication	Eric Schonthal
0.0	13-Apr-11	Initial Draft	Chris Shepherd

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1. INTRODUCTION

The RFMD208x series of parts are IQ modulators taking baseband quadrature signals in and directly modulating the local oscillator.

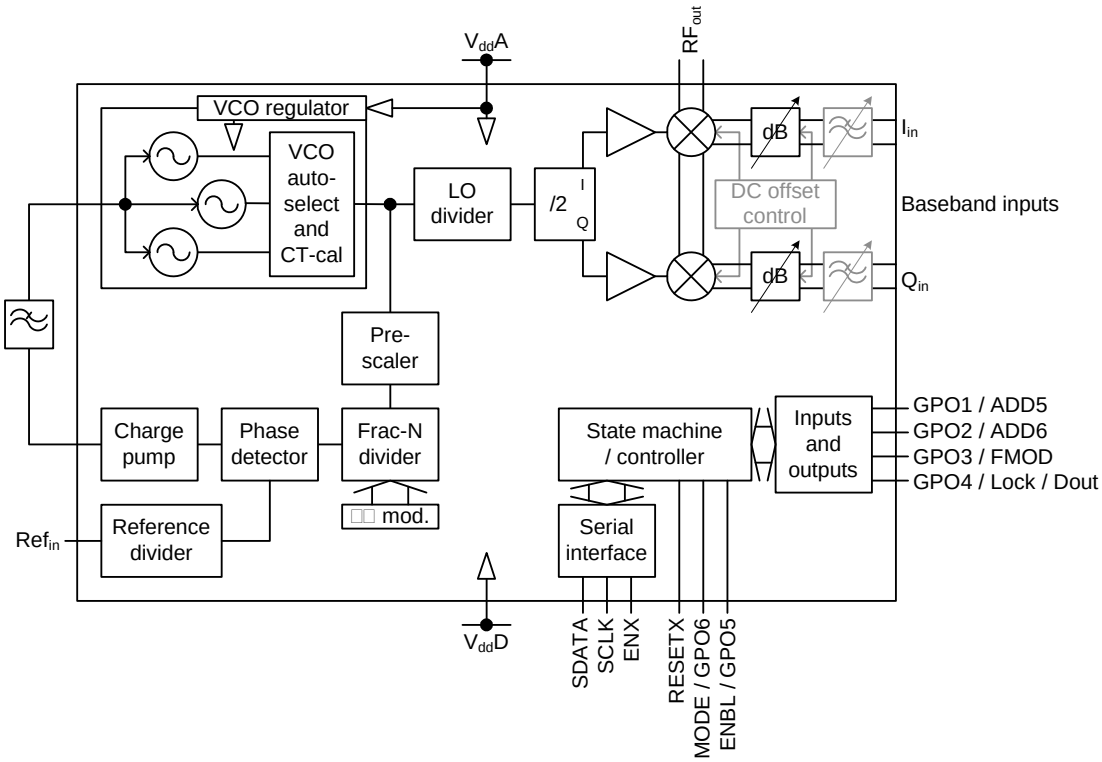
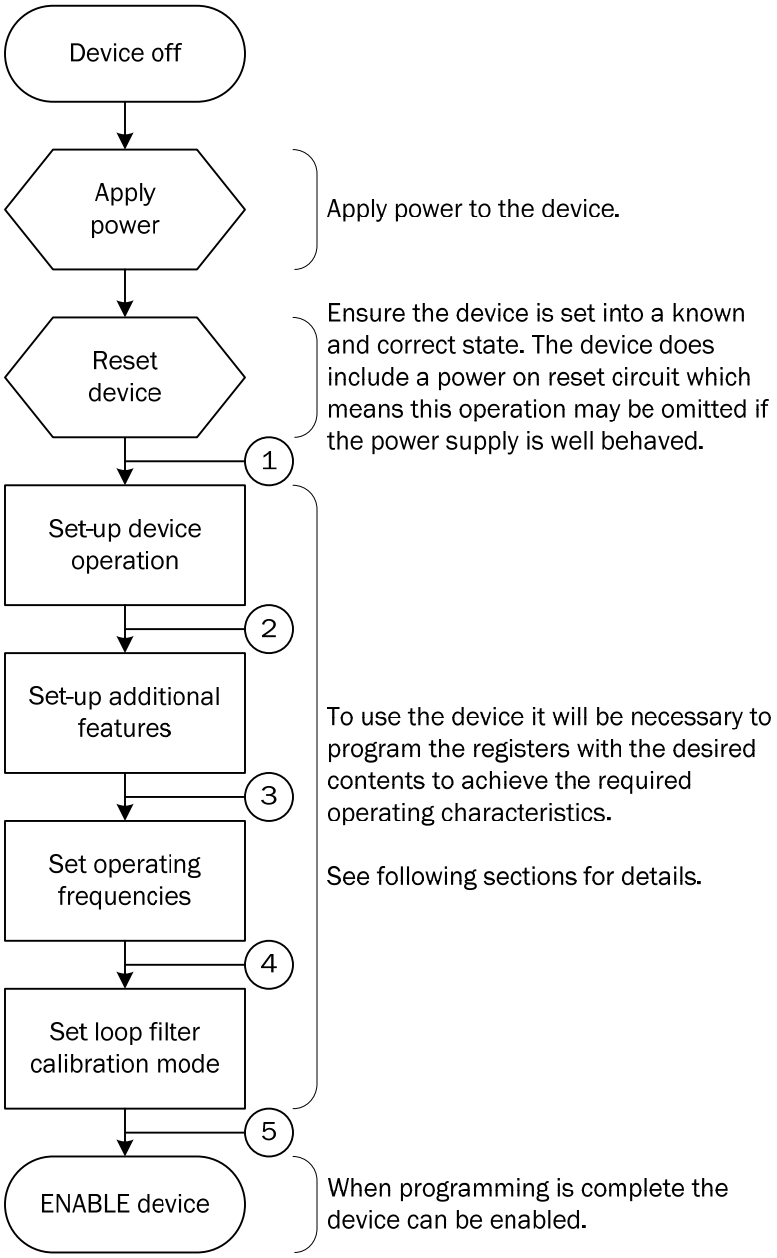
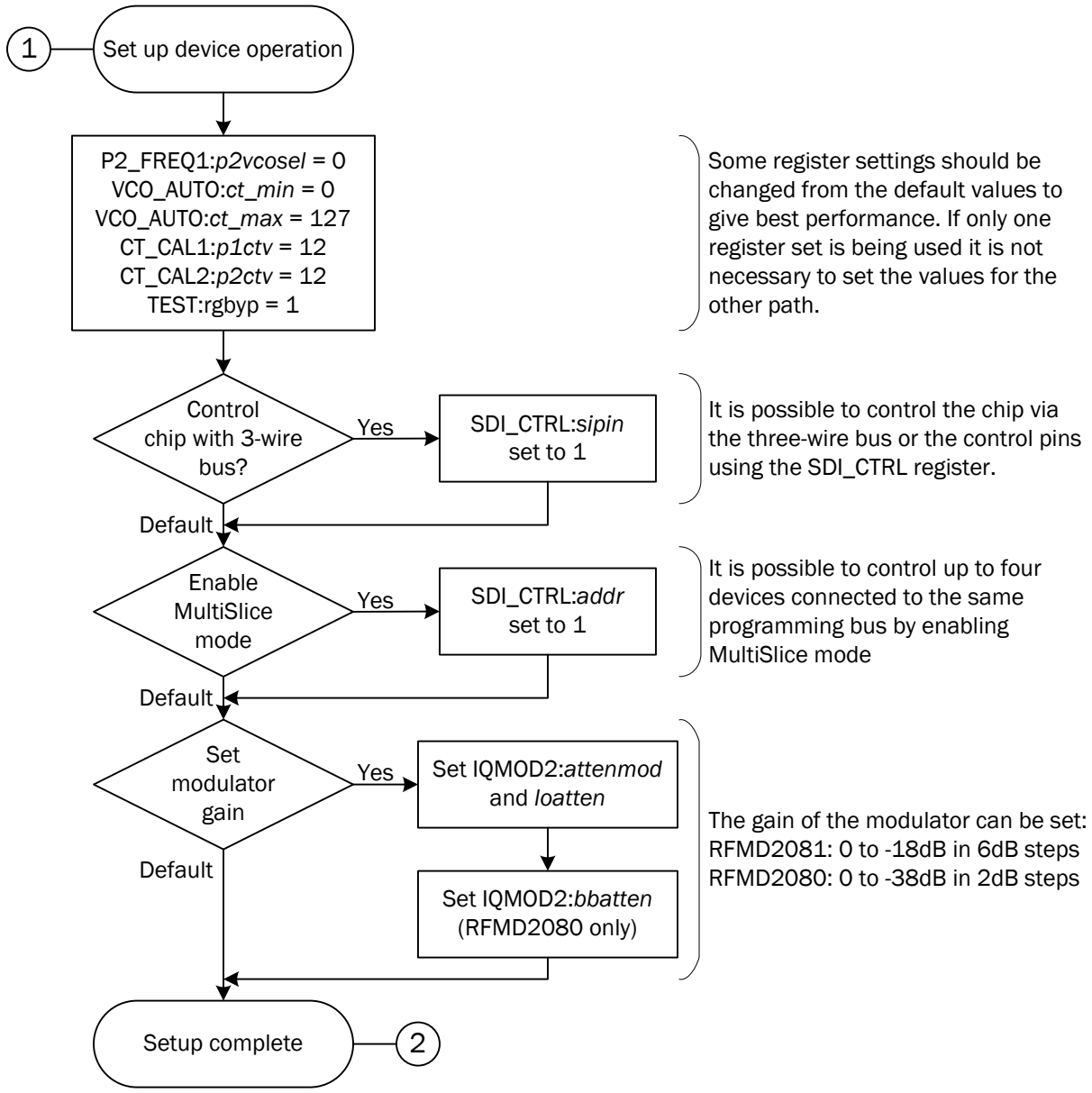


Figure 1. Modulator block diagram, showing the additional features of the RFMF2080 part

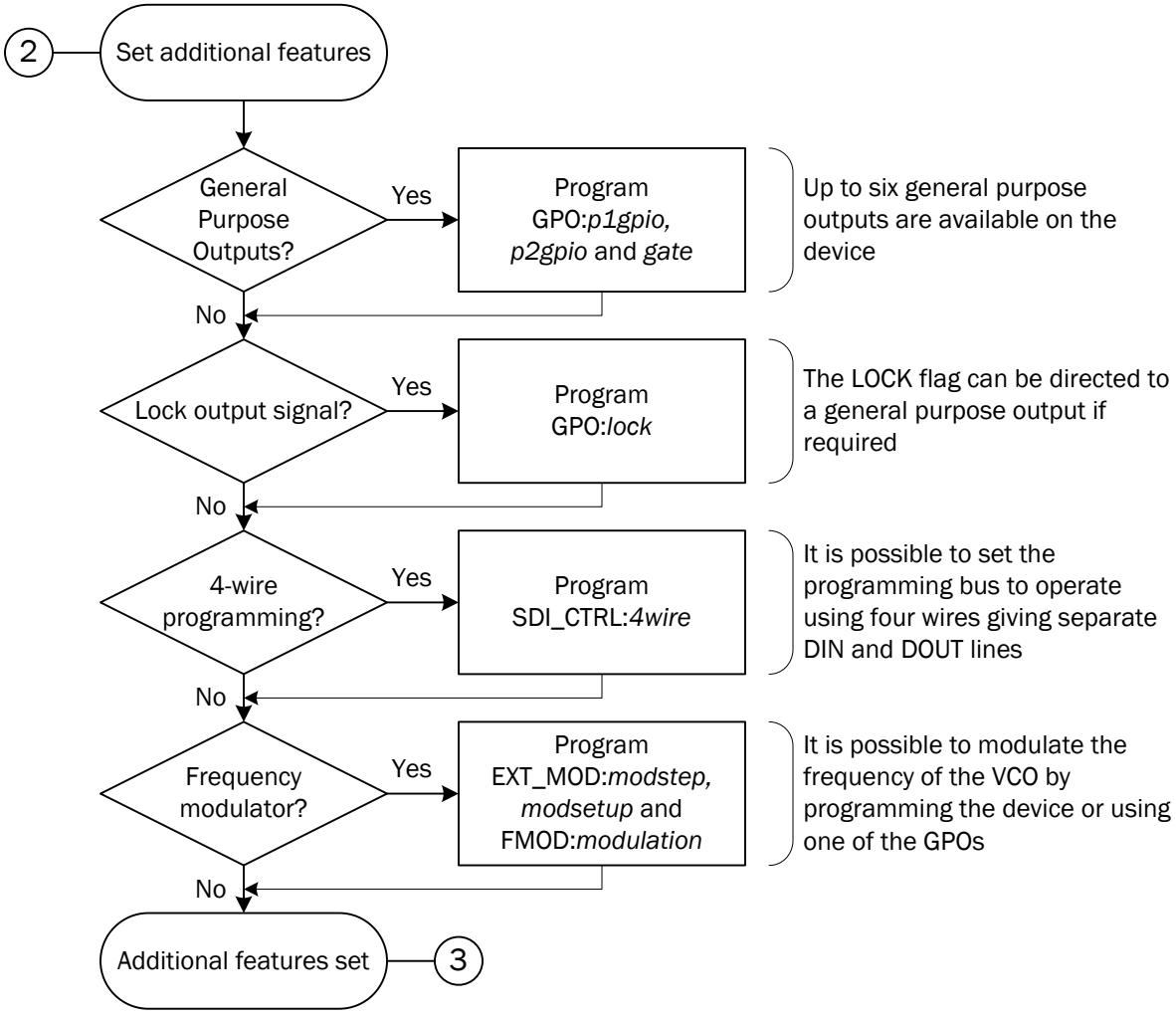
2. PROGRAMMING THE DEVICE



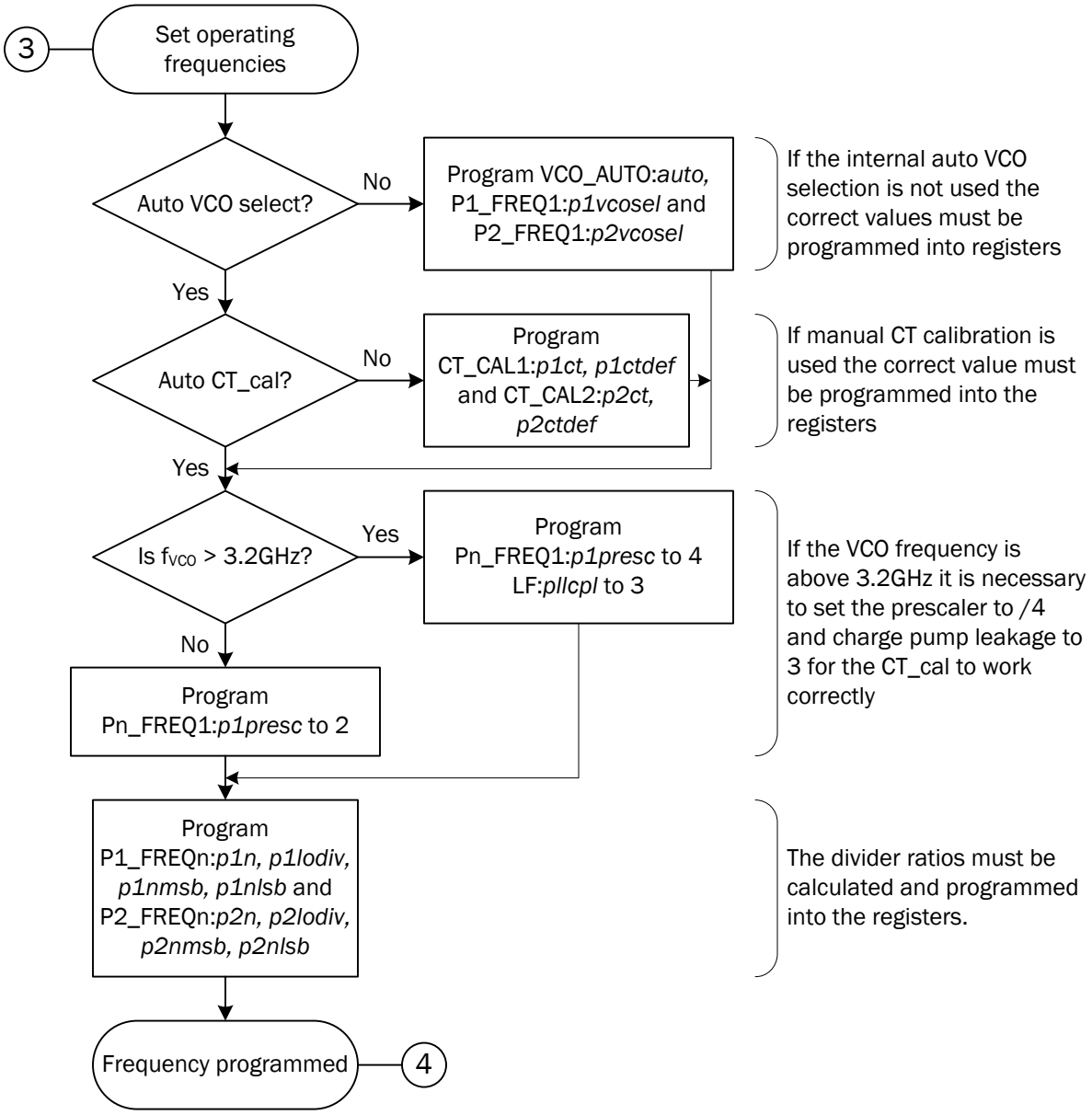
2.1 SET UP DEVICE OPERATION



2.2 SET ADDITIONAL FEATURES



2.3 SET OPERATING FREQUENCIES



2.3.1 Calculating Divider Values

There are four dividers on the chip controlling the local oscillator frequency: the LO divider, the modulator divider (IQ generator), the N-divider and its associated prescaler. The prescaler is required to restrict the input frequency to the N-divider to a maximum frequency of 1.6GHz. This is illustrated in the simplified block diagram of the synthesizer shown below.

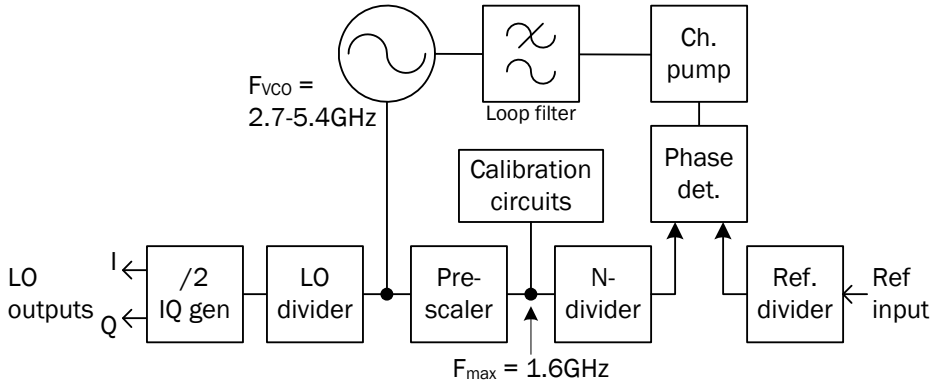


Figure 2. Simplified block diagram of the frequency synthesizer

The divider values should be calculated in the following order:

1. The LO divider (*lo_div*)
2. The N-divider (*n*, *nummsb*, *numlsb*)

$n\_lo = INT(\log_2(f_{VCOmax} / (2.f_{LO})))$

lodiv $= 2^{n\_lo}$

$f_{VCO} = 2 * lo\_div * f_{LO}$

fbkdiv $= 2\ (f_{VCO} < 3.2GHz)$

$= 4\ (f_{VCO} > 3.2GHz)$

$n\_div = f_{VCO} / fbkdiv / f_{PD}$

n $= INT(n\_div)$

nummsb $= INT(2^{16} * (n\_div - n))$

numlsb $= INT(2^8 * (2^{16}*(n\_div - n) - nummsb))$

For example an LO of 314.159265MHz with a 26MHz reference frequency would be calculated as follows:

$n\_lo = INT(\log_2(5600 / (2 * 314.159265))) = INT(\log_2(8.9126768234)) = 3$

lodiv $= 2^{n\_lo} = 8$

$f_{VCO} = 2 * lo\_div * f_{LO} = 5026.548240MHz$

fbkdiv = 4

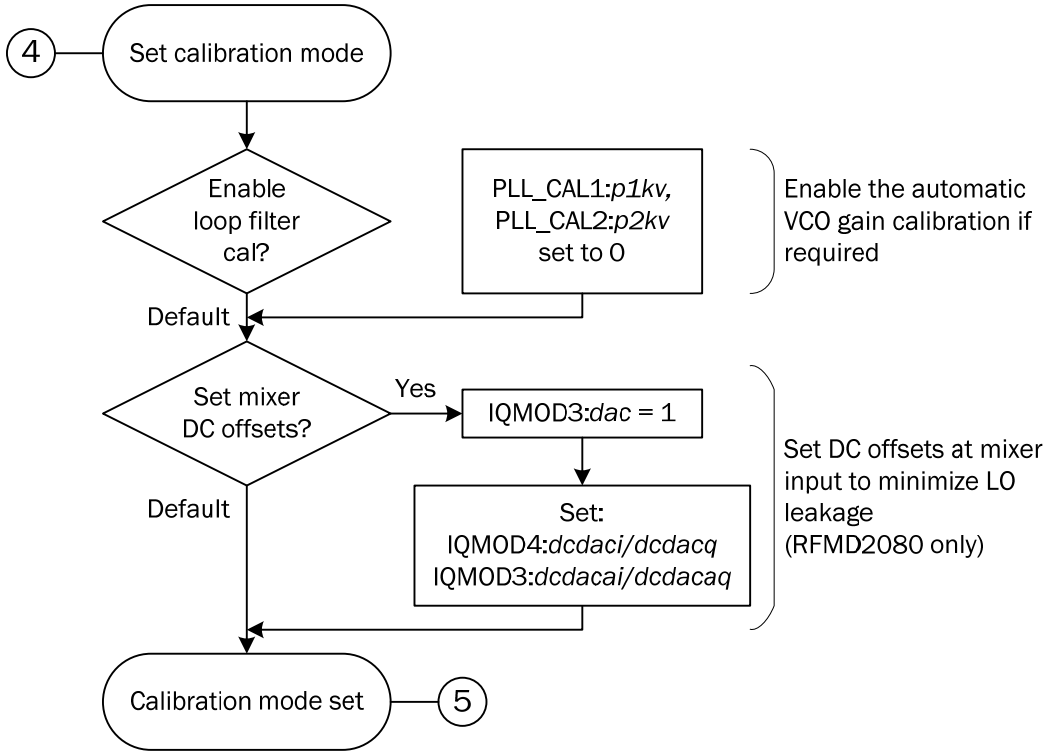
n_div = f_{VCO} / 4 / f_{PD} = 5026.54824 / 4 / 26 = 48.3321946154

n = INT(n_div) = 48 (0x030)

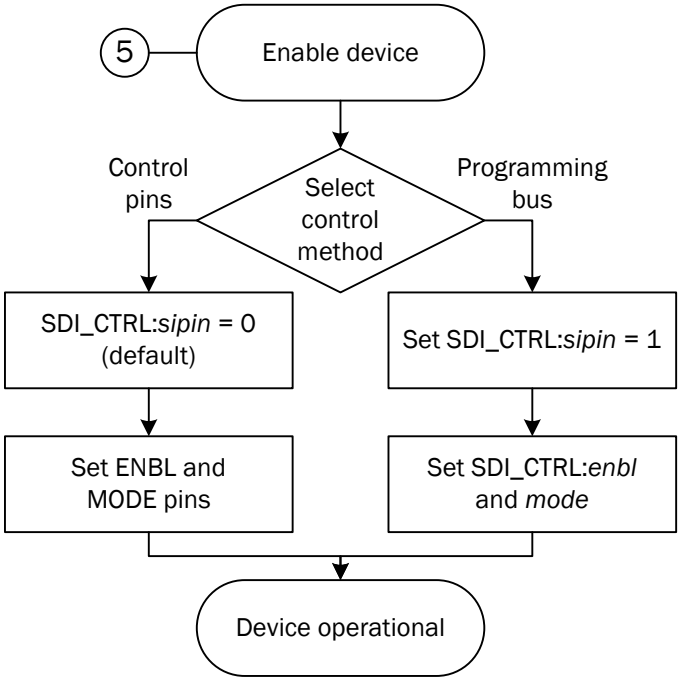
nummsb = INT(2^{16} * (n_div – n)) = 21770 (0x550A)

numlsb = INT(2^{8} * **(**2^{16}*(n_div – n) - nummsb**)**) = 181 (0x85)

2.4 SET LOOP FILTER CALIBRATION MODE



2.5 ENABLE DEVICE



2.5.1 Optimizing Phase Noise

For optimum VCO phase noise the prescaler divider should be set to divide by 2. If the VCO frequency is greater than 4GHz it is necessary to set the ratio to 4 to allow the CT cal algorithm to work. After the device is enabled the divider values can be reprogrammed with the prescaler divider ratio of 2 and the new n, nummsb and numlsb values. Taking the previous example of an LO of 314.159265MHz:

fbkdiv = 2

n_div = f_{VCO} / 2 / f_{PD} = 5026.54824 / 2 / 26 = 96.66438923

n = INT(n_div) = 96 (0x060)

nummsb = INT(2^{16} * (n_div – n)) = 43541 (0xAA15)

numlsb = INT(2^{8} * **(**2^{16}*(n_div – n) - nummsb**)**) = 106 (0x6A)

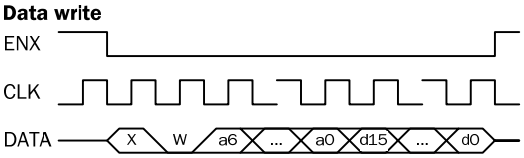
These new values would be programmed into the device since the VCO frequency is unaffected the CT_cal value will be correct.

3. SIGNALS AND TIMING

Three wires are used to program the device: ENX, CLK and Data. There is a four wire read operation which separates the read and write data paths.

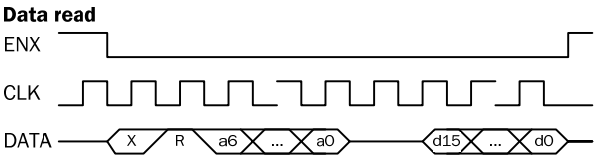
3.1 WRITE OPERATION

The first rising edge of the CLK signal resets the internal state machine; this rising edge must be sent before the ENX signal is set low. The ENX signal is held low for the duration of the write operation. The data stream is clocked into the device on the rising edge of CLK. The first data bit is a 'do not care' (X) bit, followed by the R/W bit, seven address bits and 16 data bits.

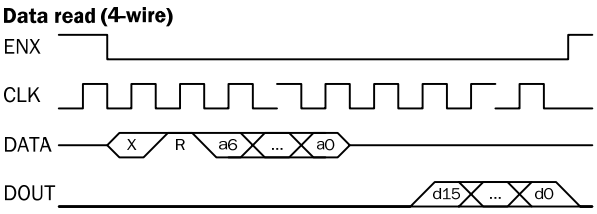


3.2 READ OPERATION

The first rising edge of the CLK signal resets the internal state machine; this rising edge must be sent before the ENX signal is set low. The ENX signal is held low for the duration of the read operation. The X, R/W and address bits are clocked into the device on the rising edge of CLK. After a period of 1.5 clock cycles during which the DATA line should become high impedance and be ready to receive data from the IQ Modulator chip, the 16 data bits are then clocked out of the IQ Modulator chip on the falling edge of CLK.

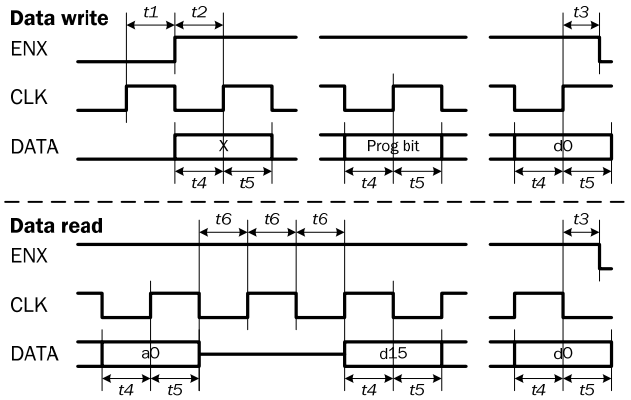


If desired it is possible to configure the device so that the data output signal is clocked out of a different pin making it possible to read the IQ Modulator device without needing to turn the DATA pin into an input. During the address write operation the DOUT pin is held low. The data is then clocked out of the IQ Modulator device on the falling edge of CLK as described above.



3.3 CRITICAL TIMING

The figures below shows the timing constraints for read and write operations.



State machine

t1	Reset time	>20ns
t2	Setup time	>20ns
t3	Hold time	>20ns

Data

t4	Setup time	>20ns
t5	Hold time	>20ns

Read/write

t6	Turn around	$> \frac{500}{19.2}$ ns

4. REFERENCES

- RFMD web site (http://www.rfmd.com)
- IQ Modulator web site (http://rfmd.com/products/IntSynthMixer/)
- IQ Modulator Evaluation Board and GUI User Guide
- IQ Modulator Register Map and Programming Guide